SAULT COLLEGE OF APPLIED ARTS AND TECHNOLOGY

SAULT STE. MARIE, ONTARIO

COURSE OUTLINE

COURSE TITLE:	ELECTRONIC CIRCUITS 1		
CODE NO. :	ELN109	**SEMESTER:**	TWO
PROGRAM:	ELECTRICAL ENGINEERING TECHNICIAN • Process Automation • Process Automation and Trades • Power Generation		
AUTHOR:	ED SOWKA		
DATE:	JANUARY 2013	**PREVIOUS OUTLINE DATED:**	JANUARY 2012
APPROVED:	*"Corey Meunier"* **CHAIR**		_____ **DATE**
TOTAL CREDITS:	5		
PREREQUISITE(S):	ELN100		
HOURS/WEEK:	5		

I. COURSE DESCRIPTION:

This course is a detailed study BJTs, JFETs, MOSFETs and OPAMPs as well as applications of these devices including transistor amplification, switching, timing circuits and OPAMP applications. This course will focus on operational analysis and troubleshooting of circuits employing these devices. Hands on skills will be reinforced in the laboratory component of this course, which includes device testing, circuit assembly, testing and troubleshooting.

II. LEARNING OUTCOMES AND ELEMENTS OF THE PERFORMANCE:

Upon successful completion of this course, the student will demonstrate the ability to:

1. Understand the construction and operation of a Bipolar Junction Transistor (BJT)

Potential Elements of the Performance:

- Describe the construction of a bipolar junction transistor (BJT) and the difference between the npn and pnp transistors.
- Describe the operation of a transistor in the active, cutoff and saturation regions and how to bias the transistor accordingly.
- Describe the transistor as a current-controlled device and state the relationship among the three terminal currents.
- Define beta and use it in transistor current calculations.
- Using a specification sheet, list the parameters and operating characteristics of different transistors.
- Describe how to test transistors in and out of circuit with an analog or digital meter.

2. Analyze, assemble, test and troubleshoot various BJT biasing configurations.

Potential Elements of the Performance:

- State the purpose of dc biasing for transistor circuits.
- Identify and analyze common transistor biasing circuits.
- Plot the dc load line for an amplifier and explain what the Q-point represents.
- Define and Calculate the Q-Point, Saturation and Cutoff.
- Describe, analyze and calculate the operation of a base-bias circuit, and explain why this bias is used when you require the transistor to act as a switch.
- Describe, analyze and calculate the operation of an emitter-feedback bias circuit.
- Describe, analyze and calculate the operation of a voltage-divider biasing circuit.
- Assemble and test biasing circuits using proper test equipment.
- Correctly use common test equipment in the analysis and troubleshooting of transistor circuits.

- Analyze, test and troubleshoot, transistor switching circuits and amplifiers.
- Identify and understand the operation of other transistor configurations including Darlington

3. Understand the operation of basic transistor amplifiers.

Potential Elements of the Performance:

- Identify and compare various Amplifier classes.
- List the fundamental ac properties of amplifiers.
- Derive the ac equivalent for a class A amplifier.
- Explain and calculate the effects of input and output impedance on voltage gain.
- Perform a complete mathematical dc and ac analysis of a voltage divider bias class A amplifier.
- Assemble and test a single stage amplifier for proper dc and ac voltages.
- Troubleshoot a multi-stage amplifier in a safe and proper manner.

4. Understand the characteristics, operation, biasing, and testing of JFETs and MOSFETs.

Potential Elements of the Performance

- Identify the two types of JFETs and describe the construction and operation of each.
- Describe and analyse the different types of JFET biasing circuits.
- Compare FET characteristics, advantages and disadvantages with BJT's
- Identify the two types of MOSFETs and describe the construction and operation of each.
- Describe and analyse the different types of MOSFET biasing circuits
- Assemble, test and troubleshoot different JFET and MOSFET circuits.

5. Understand the operation, characteristics and applications of Operational Amplifiers (OPAMPS)

Potential Elements of the Performance:

- Describe the operational amplifier.
- Explain IC identification of an OPAMP.
- Explain the term differential amplifier.
- Describe the operation of a discrete differential amplifier.
- Using a specification sheet, list and understand the operating and electrical characteristics of OPAMPS.
- Describe, analyse and calculate the operation of common OPAMP circuits including Inverting, Non-Inverting, Follower, Comparator, Schmitt Trigger.
- Assemble, test and troubleshoot common OPAMP circuits.

III. TOPICS:

1. Bipolar Junction Transistors, Circuits and Applications.
2. JFETs, MOSFETs and their applications.
3. Operational amplifiers and their applications

IV. REQUIRED RESOURCES/TEXTS/MATERIALS:

- Introductory Electronic Devices and Circuits (Conventional Flow Version) Seventh Edition – Robert T. Paynter – Prentice Hall.
- 1st Year Parts Package / DMM
- Assorted handouts as required
- Internet Resources

V. EVALUATION PROCESS/GRADING SYSTEM:

The final grade will be derived as follows:

- Theory - Tests (3) and Quizzes = 45%
- Lab - Practical tests and reports = 50%
- 1st Semester Review Test = 5%
- TOTAL =100%

NOTE: You must obtain a minimum mark of 50% in both the Theory portion and the Lab portion of the course. Failing to do so, will result in an overall failing grade (F).

See Special Notes Section VI
for further details affecting final grade.

The following semester grades will be assigned to students in other than postsecondary courses:

Grade	Definition	*Grade Point Equivalent*
A+	90 – 100%	4.00
A	80 – 89%	
B	70 - 79%	3.00
C	60 - 69%	2.00
D	50 – 59%	1.00
F (Fail)	49% and below	0.00

CR (Credit)	Credit for diploma requirements has been awarded.
S	Satisfactory achievement in field /clinical placement or non-graded subject area.
U	Unsatisfactory achievement in field/clinical placement or non-graded subject area.

X	A temporary grade limited to situations with extenuating circumstances giving a student additional time to complete the requirements for a course.
NR	Grade not reported to Registrar's office.
W	Student has withdrawn from the course without academic penalty.

VI. SPECIAL NOTES:

Attendance:
Sault College is committed to student success. There is a direct correlation between academic performance and class attendance; therefore, for the benefit of all its constituents, all students are encouraged to attend all of their scheduled learning and evaluation sessions. This implies arriving on time and remaining for the duration of the scheduled session.

It is the departmental policy that once the classroom door has been closed, the learning process has begun. Late arrivers will not be granted admission to the room.

VII. COURSE OUTLINE ADDENDUM:

The provisions contained in the addendum located on the portal form part of this course outline.

Additional Criteria;

- Attendance to lab activities is compulsory, unless discussed with the instructor in advance of the absence and the absence is for a medical or family emergency. A ***deduction of 2% per Lab missed*** will be imposed on the final mark. Your attendance to all classes and your final grade are directly related and as such, it is strongly recommended to attend all scheduled Theory Classes / Tutorials.

- Any student that is absent for any test (for a legitimate emergency) will be required to provide a doctors' note immediately upon returning. Failing to do so will result in a grade of 0% being assigned to the missed test. It is the students' responsibility to contact the college and/or Professor. Test dates will be provided to the students, a minimum of 2 weeks in advance of the test date.

- Tests, quizzes and other activities will not be scheduled on an individual basis, unless it is for a medical or family emergency.

- Disruptions to theory classes, such as lateness, are not acceptable and will be dealt with on an individual basis. Students exhibiting chronic lateness or absenteeism will be required to meet with the Dean, and will be placed on academic probation.

- The use of Electronic Recording Devices is prohibited unless individual permission is obtained from the instructor. The use of Cell Phones during scheduled classes is prohibited. Turn off all Cell Phones before attending class.

- ***Laboratory Reports*** shall be subject to the handout and or criteria given at the start of the semester by the Professor. All Lab Reports are due ***before*** the start of the following weeks Scheduled Lab Class (or alternate indicated deadline) unless otherwise stipulated by the instructor. A ***deduction of 20%*** will be assessed for late submissions within the first 24 hour period following the deadline. A ***deduction of 50%*** will be assessed if submitted after this initial 24 hours, but before 48 hours. Reports submitted after 48 hours of the specified deadline will be graded as 0% (Weekends included in all deadline requirements).

- **All Lab reports must be submitted. Failing to complete and submit any labs, will result in an overall grade of "F".**

Lab Reports are graded based on the following:

- 1) Ability to follow instructions, 2) Ability to follow specific procedures, 3) Ability to use test equipment to obtain data, 4) Accuracy of data, 5) Ability to use required software, 6) Ability to adhere to established deadlines, 7) Ability to draw conclusions based on objectives, 8) Ability to produce a technical report as specified.

- ***Incomplete submissions*** will be returned to the student and will not be graded until such a time as they are completed. The maximum mark that can be obtained for incomplete labs re-submitted will be 50%. Incomplete reports must be re-submitted within 5 days from the date of being returned to the students (not the day the student picks up the graded report). Incomplete reports handed in after the 5 day period, will not be accepted and be graded 0% and as such will be considered an outstanding report.

- **All Lab Reports must be submitted in a Duo-Tang cover (No Binders) unless otherwise noted. No loose papers will be accepted and as such will be graded 0%.**

- Theory Tests will not be returned. Students will be given the opportunity to review / correct the test material.